
Chapter 6 — DTI/PRI Maintenance

Maintenance overview

From a maintenance perspective, Option 11 DTI/PRI operation consists of these major aspects:

- hardware and software states
- near-end and far-end status
- link and/or span integrity
- clocking status
- frame alignment

Option 11 PRI operation is monitored and reported on through maintenance messages, out-of-service alarms, and circuit card faceplate LEDs. Bantam monitor jacks are located on the faceplate of the NTAK09.

Option 11 maintenance provides several tools, either manual or automatic, for maintaining effective PRI operation. These tools are service change and maintenance commands that are accessible through the software overlays and resident diagnostic routines.

Monitoring Option 11 DTI/PRI operation

Maintenance messages

The following sections describe the maintenance messages that may appear on the Option 11 maintenance TTY as a result of DTI or PRI operation.

D-Channel status and error conditions are reported as DCH messages. PRI status and error conditions are shown in Table 31. (Additional information on PRI and DCH messages can be found in the Option 11 Software Guide.)

Table 31
Maintenance messages

Message	Meaning
DTA	Digital Trunk Alarms (Resident Monitor)
DTC	Resident CC Monitor
DTI	Digital Trunk Interface and CC (LD60)
PRI	Primary Rate Interface

Message descriptions

Maintenance messages provide near and far end switch status. Both service and service acknowledge messages are supported on PRI B-channels and ISL channels.

Service and service acknowledge messages for B-channels and ISL channels are supported between:

- Meridian 1 to Meridian 1: ISL and PRI
- Meridian 1 to DMS-100: PRI only
- Meridian 1 to DMS-250: PRI only
- Meridian 1 to AT&T ESS4 and ESS5: PRI only

The statuses reported by the service and service acknowledge messages for B-channels and ISL channels are:

- in-service
- maintenance
- out-of-service.

Near-end and far-end sub-categories are defined for each maintenance status. See the table below for possible combinations of near-end and far-end statuses, and the channel capability for each status. When the near-end and far-end status does not match, the more severe maintenance status takes effect over the less severe maintenance status.

Table 32
Maintenance message and status combinations

Near End Status	Far End Status	B or ISL Channel capability
In-service	In-service	Incoming and outgoing call allowed
In-service	Maintenance	Incoming calls allowed only
In-service	Out-of-service	Not allowed to use
Maintenance	N/A	Not allowed to use
Out-of-service	N/A	Not allowed to use

Note: Enabling/Disabling of Service Messages must be coordinated between the two ends. Enabling Service Messages at one end and not the other will result in B-channels being placed out-of-service.

Message functions

Service messages are used to monitor the following:

- D-Channel establishment
- D-Channel sanity polling
- B-channel or ISL channel status change
- Channel status audit.

D-Channel establishment

When the D-Channel establishes, the B-channel status is supported by sending service messages for each B-channel controlled by a D-Channel. This messaging allows the far end to synchronize its channel states. The service messages are sent when the D-Channel is brought up automatically by the system or manually by using LD 96.

D-Channel sanity polling

If a D-Channel has been idle for 30 seconds, a service message is sent to poll the sanity of the link. The service message is sent regardless of whether the near end is configured as master or slave.

B-channel or ISL channel status change

Whenever there is a status change for a B-channel or an ISL channel, the new status is reported to the far end via a service message. Status change can occur through service change or maintenance operations, such as the addition or deletion of a channel in LD 14, or disabling of the associated loop, shelf, card or unit in LD 30, LD 32, LD 36, LD 41 or LD 60.

Channel status audit

LD 30 is enhanced to allow channel status audit to be initiated. The channels associated with each D-Channel are examined and their status is reported to the far end via service messages.

Activating service messages

You activate the service messages in LD 96 on a per D-Channel basis. The backup D-Channel (if equipped) automatically operates in the same mode as the primary D-Channel. The commands are listed in Table 33.

Table 33
D-Channel messages

Command	Description
ENL SERV N	turns on the support of service and service acknowledge messages for DCH link N.
DIS SERV N	turns off the support of service and service acknowledge messages for DCH link N.
STAT SERV (N)	displays the current service and service acknowledge message SERV setting for individual DCH N or DCH.

When configuring these messages, the SERV command should only be enabled if both switches are equipped with a minimum of X11 release 15 software. The status of Service Messages for each D-Channel is saved by Equipment Data Dump (EDD), and is set automatically after each system load.

Note: D-Channels on each side of the link must be disabled in order to enable service messages.

Alarms

DTI/PRI Yellow Alarm (remote alarm)

A yellow alarm on the Option 11, indicated by the state of the YEL LED on the NTAK09 circuit card, is notification of a red alarm at the far end (remote end). The fact that the NTAK09 is receiving the yellow alarm pattern indicates that there is a T1 connection, but the far end is not ready.

It is possible, however, that the T1 connection is one-way only — that is, receiving only, since this end is receiving the alarm. The yellow alarm is transported in one of two ways: using digit-2 or the facility data link (DG2 or FDL).

When the NTAK09 receives a yellow alarm, the channels are placed into the maintenance busy state.

Each time a yellow alarm is generated, a counter is incremented. When the yellow alarm 24-hour threshold (prompt RALM in LD 73) is reached, the NTAK09 must be restored to service manually.

DTI/PRI Red Alarm (local alarm)

A red alarm (local alarm) indicates that the digital trunks or B-channels have been taken out of service (OOS) due to a loss of frame alignment lasting more than 3 seconds, or due to some facility performance OOS threshold being exceeded.

Maintenance and OOS messages are discussed later in this chapter.

NTAK09 Faceplate LEDs

The NTAK09 circuit card has a total of seven faceplate LEDs. Five of the LEDs are directly associated with the operation of the NTAK09 circuit card.

The remaining two LEDs are associated with the optional daughterboards. The first of these LEDs is used to indicate the status of the NTAK20 Clock Controller daughterboard. The second indicates the state of the NTAK93 D-Channel interface daughterboard, when this board is present.

Table 34 provides a summary of the NTAK09 faceplate LEDs.

Table 34
NTAK09 faceplate LEDs

Affected circuit card	LED	State	Definition
NTAK09	DIS	On (Red)	The NTAK09 circuit card is disabled.
		Off	The NTAK09 is not in a disabled state.
NTAK09	ACT	On (Green)	The NTAK09 circuit card is in an active state. No alarm states exist, the card is not disabled, nor is it in a loopback state.
		Off	An alarm state or loopback state exists, or the card has been disabled. See the other faceplate LEDs for more information.
	RED	On (Red)	A red-alarm state has been detected.
		Off	No red alarm.
	YEL	On (Yellow)	A yellow alarm state has been detected.
		Off	No yellow alarm.
	LBK	On (Green)	NTAK09 is in loop-back mode.
		Off	NTAK09 is not in loop-back mode.
NTAK20	CC	On (Red)	NTAK20 is equipped and disabled.
		On (Green)	NTAK20 is equipped and is either locked to a reference or is in free run mode.

Affected circuit card	LED	State	Definition
		Flashing (Green)	NTAK20 is equipped and is attempting to lock (tracking mode) to a reference. If the LED flashes continuously over an extended period of time, check the CC STAT in LD60. If the CC is tracking this may be an acceptable state. Check for slips and related clock controller error conditions. If none exist, then this state is acceptable, and the flashing is identifying jitter on the reference.
		Off	NTAK20 is not equipped.
NTAK93 NTBK51	DCH	On (Red)	NTAK93 or NTBK51 is switched on and disabled.
		On (Green)	NTAK93 or NTBK51 is switched on and enabled, but not necessarily established.
		Off	NTAK93 or NTBK51 is switched off (by switch SW1).

Note: Only one of the five NTAK09 related LEDs should be on at any one time.

Monitor Jacks

The NTAK09 has two bantam jacks (RCV and XMT) located on its faceplate. They may be used to monitor the performance of the carrier in the receive and transmit direction. The jacks allow the convenient connection of external T-1 test equipment and ISDN protocol analyzers. Such external test equipment is not normally required for the operation and maintenance of DTI/PRI.

Using Option 11 DTI/PRI maintenance tools

Maintenance commands

Tables 35, 36 and 38 provide quick reference lists of important DTI/PRI commands.

WARNING

You must disable the D-Channel and clock-controller daughterboards before unseating circuit cards, otherwise the system will INIT and momentarily interrupt call processing.

WARNING

Extreme care must be taken when enabling the D-Channel message monitoring option due to the possible heavy volume of messages during normal traffic. Use this command only during very light or no traffic conditions for trouble-shooting purposes. Remember to disable the monitoring tool when you are finished — it does not time out. Monitor enabled status is saved by EDD and will remain enabled even after a SYSLOAD.

The port (TTY) performing the monitoring **MUST** have MTC and BUG programmed.

Table 35
DTI/PRI commands (LD 60)

Command	Action
DISI C	disable DTI/PRI card when idle
DISL C	force disable DTI/PRI card
ENLL C	enable DTI/PRI card
LCNT (C)	list alarm counters
RCNT (C)	reset alarm counters
SLFT (C)	do DTI/PRI self-test
STAT (C)	list DTI/PRI status
RLBK	remote loopback

Table 36
D-Channel commands (LD 96)

Command	Action
DIS DCH N	disable DCHI port N
DIS MSGI N	disable monitoring of incoming D-Channel messages on link N Monitor remains active until disabled.
DIS MSGO N	disable monitoring of outgoing D-Channel messages on link N Monitor remains active until disabled.
DIS AUTO N	disable autorecovery of the D-Channel. Hardware may still respond to recovery initiated from the far end.
ENL AUTO N	enable autorecovery of the D-Channel. Software will periodically command hardware to attempt to establish the layer 2 link.
ENL DCH N	enable DCHI port N
ENL MSGI N	enable monitoring of incoming D-Channel messages on link N Use only under light traffic.
ENL MSGO N	enable monitoring of outgoing D-Channel messages on link N Use only under light traffic.
EST DCH N	establish D-Channel N
PLOG DCH N	print D-Channel statistics log N

Command	Action
RLS DCH N	release D-Channel N
SDCH	release a D-Channel and switch D-Channels
RST DCH N	reset D-Channel N
STAT DCH (N)	print D-Channel status (link status)
STAT MSGI (N)	print incoming message monitor status
STAT MSGO (N)	print outgoing message monitor status
TEST-100/101/200/201	see DCH tests in NTP
STAT SERV	Print the current service and service acknowledge message for DCHI N
ENL SERV N	enable service messages for DCHI N
DIS SERV N	disable service messages for DCHI N

Table 37
Downloadable D-channel (DDCH) commands (LD 96)

Command	Action
DIS MSDL X (ALL)	disable DCHI card X
ENL MSDL X (FDL, ALL)	enable DCHI card X, with or without Force Download
RST MSDL X	Reset MSDL card X
STAT MSDL X (X (full))	Get MSDL status X, or a "FULL STATUS"
SLFT MSDL X	Execute a self test on MSDL card X
DIS LLB X	Disable local loop back on MSDL DCH X
DIS RLB X	Disable remote loop back on MSDL DCH X
DIS TEST X	Disable Test mode on MSDL DCH X
ENL LLB X	Enable local loop on MSDL DCH X
ENL RLB X	Enable remote loop on MSDL DCH X
ENL TEST X	Enable Test mode on MSDL DCH X
PCON DCH X	Print configuration parameters on MSDL DCH X
PMES DCH X	Print incoming layer 3 messages on MSDL DCH X
PTRF DCH X	Print traffic report on MSDL DCHX

TEST LLB X	Start local loop back test on MSDL DCH X
TEST RLB X	Start remote loop back test on MSDL DCH X

Note: “X” represents the D-Channel device number

D-channel status and error conditions are reported as DCH messages. These messages can be found in the Option 11 *Software guide*.

Table 38
Clock Controller commands (LD 60)

Command	Action
DIS CC N	disable clock controller N
ENL CC N	enable clock controller N
SSCK N	status of clock controller N
TRCK XXXX XXXX can be: PCK SCLK FRUN	set clock controller tracking. track primary clock reference source track secondary clock reference source free run mode

NTAK09 DTI/PRI power on self-test

When power is applied to the NTAk09 DTI/PRI circuit card, the card performs a self test. The LEDs directly associated with the NTAk09 circuit card are DIS, ACT, RED, YEL, and LBK. The clock controller LED is also included in the power on self test (see below).

Table 39 provides the state of the NTAk09 LEDs during the self-test procedure.

Table 39
NTAk09 LED states during self-test

Action	LED State
Power up system	Top five LEDs on for eleven seconds
Self-test in progress	Top five LEDs go off for one second If the self-test passes, the top five LEDs flash on and off three times. If the self-test detects a partial failure, the top five LEDs flash on and off five times When the self-test is completed, the LEDs go to their appropriate states (see Table 34)

NTAk20 power on self-test

The clock controller daughterboard LED is the second LED from the bottom on the faceplate of the NTAk09 DTI/PRI card.

When power is applied to the NTAk20 clock controller, the LED is initially off for two seconds. If the self-test passes, the LED turns red and flashes on and off twice.

When the self-test is completed, the LED will remain red until the clock controller is enabled. When enabled, the clock controller LED will turn green or flashing green. (See Table 34).

NTAk93 self-test

The NTAk93 DCHI daughterboard LED is the bottom LED on the faceplate of the NTAk09 DTI/PRI card.

The NTAK93 DCHI daughterboard does not perform a self-test when power is applied to it. When power is applied, it will turn red and remain steadily lit, indicating the DCH is disabled. When the DCH is enabled, the LED will turn green and remain steadily lit.

Self-tests of the NTAK93 daughterboard are invoked manually by commands in LD 96.

DTI/PRI local self-test

The local self-test, also called a local loopback test, checks speech path continuity, zero code suppression, remote alarm detection, and A & B bit signalling. This test is performed manually on a per-loop (or link- 24 channels) or per-channel basis. The local loopback test performs a local logical loopback and does not require any external loopback of the T-1 signal.

Restrictions and limitations

The DCHI and DTI/PRI must be disabled before performing the self-test on the entire DTI/PRI card. Individual channels must be disabled before performing a self test on a particular channel.

Self testing the DTI/PRI card

To perform a self test on the entire DTI/PRI card, do the following:

- 1 Disable the DCHI using LD 96:

LD 96

DIS DCH N

- 2 Disable the DTI/PRI card and run the self-test using LD 60:

LD 60

DISL C

SLFT C (entire card)

Self testing individual channels

Follow the same procedure as above, but use the following commands:

DSCH C CH

SLFT C CH (specific channel)

DTI/PRI automatic local loopback test

There are two types of automatic local loopback tests:

- ATLP 0 (disable auto loop test in daily routine — LD 60)
- ATLP 1 (enable auto loop test in daily routine — LD 60).

The automatic loop test checks the same functions as the manual self test, but runs automatically as part of the midnight routines.

ATLP 0 disables one idle channel at random and performs a single channel self test. This channel cannot be specified — it is selected by software.

ATLP 1 attempts to test the whole DTI/PRI loop. If ATLP 1 finds all channels in the target link idle, it takes the whole link down and tests it. The node where the self test is being performed sends out a Yellow Alarm while the link is down.

Ensure that LD 73 TRSH RALM will not be exceeded at the far end due to automatic running of the loop test. If TRSH RALM (default=3) is exceeded at the far end, trunks will remain out of service.

ATLP 0	AUTO SELF TEST LOOP DISABLE
ATLP 1	AUTO SELF TEST LOOP ENABLE

Remote Loopback and remote self test

The remote loopback and the remote self test are performed manually per loop (or per card in Option 11).

Remote Loopback

The RLBK C command puts the DTI/PRI into loopback towards the far end so a remote self test can be performed on equipment at the far end.

Note: The DTI/PRI loop (card) being tested must be disabled.

Remote loopback test

The remote self test, also called the external loopback test, checks the integrity of the DTI/PRI through an external T-1 loopback. If the Remote Loopback command (RLBK) is executed at the far end Meridian 1/SL-1 prior to executing the Remote Self test command (RMST) at the near end, the integrity of the DS-1 facility is tested from end to end.

Note: The DTI/PRI channel or loop (card) being tested must be disabled.

Coordinating the tests

- 1** When a technician at the far end requests a remote loopback on the local Meridian 1:

- Disable the DCHI (for PRI DCHL or BCHL) using LD 96:
LD 96

DIS DCH N

- Disable the DTI/PRI card and activate remote loopback mode using LD 60:

LD 60

DISL C

RLBK C

2 To run the remote self test (external loopback test) through a loopback on the far end Meridian 1:

- Call a technician at the far end. Ask for remote loopback mode on the facility that is to be tested.
- When loopback mode at the far end is confirmed, disable the DCHI (for PRI DCHL or BCHL) using LD 96:

LD 96

DIS DCH N

- Disable the DTI/PRI card and run loopback test using LD 60:

LD 60

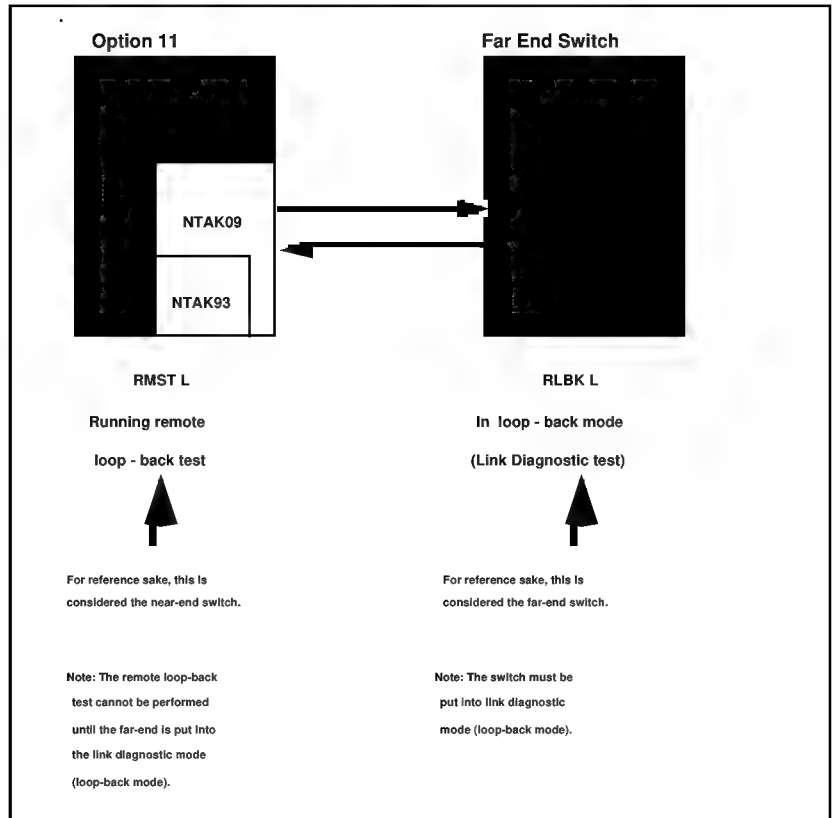
DISL C

RMST C

Note: The Remote Self test (external loopback test) can be run through any loopback that is external to the DTI/PRI card. The loopback can range from a loopback connector plugged into the NTBK04 cable to a Remote Loopback on the far end DTI/PRI, or at any point in between on the DS-1 facility.

Figure 66 shows the relationship between the remote loopback test and the link diagnostic test.

Figure 66
DTI/PRI link diagnostic and remote loopback tests



DTI/PRI error detection

Bit error rate

Bit error rate monitoring detects errors in transmission. (See Figure 67). There are two methods of bit error monitoring: bipolar violation tracking and Cyclic Redundancy Check (CRC).

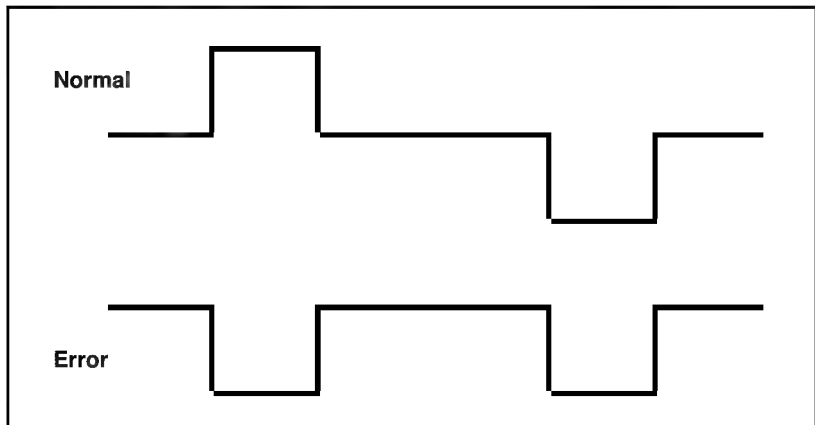
If the D2, D3 or D4 framing format is selected in overlay 17 prompt DLOP, then bipolar violation tracking is implemented. If the Extended Superframe (ESF) format is selected, CRC is implemented.

Bipolar violation (BPV) tracking

In a bipolar pulse stream, pulses alternate in polarity. A bipolar violation has occurred if, after transmission, two pulses of the same polarity are received in succession (this could be caused by an electrical disturbance such as noise).

Note: Bipolar 8 Zero Substitution (B8ZS) introduces intentional bipolar violations. The T1 equipment must treat them as such and disregard them. This explains why B8ZS can only be used if all the equipment on the T1 span (end-to-end) supports it. Otherwise the intentional BPVs take the link down.

Figure 67
Bipolar violations



Cyclic Redundancy Check (CRC)

The Extended Superframe Format (ESF) contains a checksum of all data in the frame. The receiving side uses the checksum to verify the data.

The primary difference between BPV and CRC is that bipolar violation tracking indicates errors in the local span, while CRC indicates errors on an end to end span. For example, on a satellite link, BPV only detects errors in the span between the Meridian 1 and the satellite connection. Since CRC traverses the entire span, it indicates an end-to-end bit error rate.

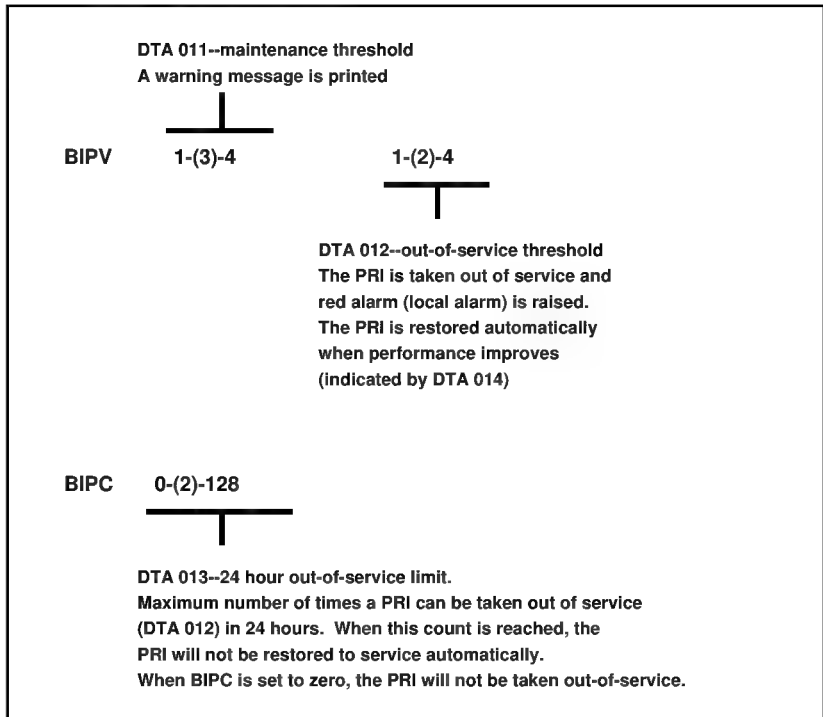
DTI/PRI hardware detects BPV or CRC errors. It sends an overflow (OVFL) message to the Meridian 1 CPU each time 1024 BPV or CRC errors are detected. Running the midnight routines prints the number of overflows and clears the counter.

Bit error rate threshold messages

There are three bit error rate thresholds set in LD 73, using one of two prompts: BIPV or BIPC. When a threshold is reached, a DTA message is produced. (See Figure 68.)

Message	Explanation
DTA011	Bit error rate maintenance threshold has been reached.
DTA012	Bit error rate out of service limit has been reached.
DTA013	Too many bit error rate out of service occurrences in the last 24 hours.

Figure 68
BIPV and BIPC thresholds



Frame slip

Digital signals must have accurate clock synchronization for data to be interleaved into or extracted from the appropriate timeslot during multiplexing and de-multiplexing operations. A frame slip is defined as the repetition of, or deletion of, the 193 data bits of a DS-1 frame due to a sufficiently large discrepancy in the read and write rates at the buffer (clocks aren't operating at EXACTLY the same speed).

When data bits are written into (added to) a buffer at a slightly *higher* rate than that at which they are being read (emptied), sooner or later the buffer overflows. This is a slip-frame deletion.

In the opposite situation, when data bits are written (added) into a buffer at slightly *lower* rate than that at which they are being read (emptied), eventually the buffer runs dry or underflows. This is also a slip-frame repetition.

Either occurrence is called a slip (or a controlled slip). The Option 11 contains a buffer large enough to hold about 2 full DS-1 frames ($193 * 2 = 386$). It is normally kept half full (1 frame). Slippage has impact on the data being transferred, as is shown in the table below, and all of the degradations shown in the table can be controlled or avoided with proper clock (network) synchronization.

Table 40
Impact of slip on service types

Service	Potential Impact
Encrypted Text	Encryption key must be resent.
Video	Freeze frame for several seconds. Loud pop on audio.
Digital Data	Deletion or repetition of Data. Possible Misframe.
Facsimile	Deletion of 4-8 scan lines. Drop Call.
Voice Band Data	Transmission Errors for 0.01 to 2 s. Drop Call.
Voice	Possible Click

Types of synchronization

Clock synchronization can be either tracking on the primary or secondary reference clock or free run (non-tracking). In LD 73 (prompts PREF and SREF), the DTI/PRI which supports the clock controller daughterboard is defined as the primary clock reference.

Another DTI/PRI may be defined as the secondary clock reference. The clock controller will synchronize from the primary or secondary's incoming pulse stream. The clock controller will in turn supply clocking to all the other DTI/PRI loops.

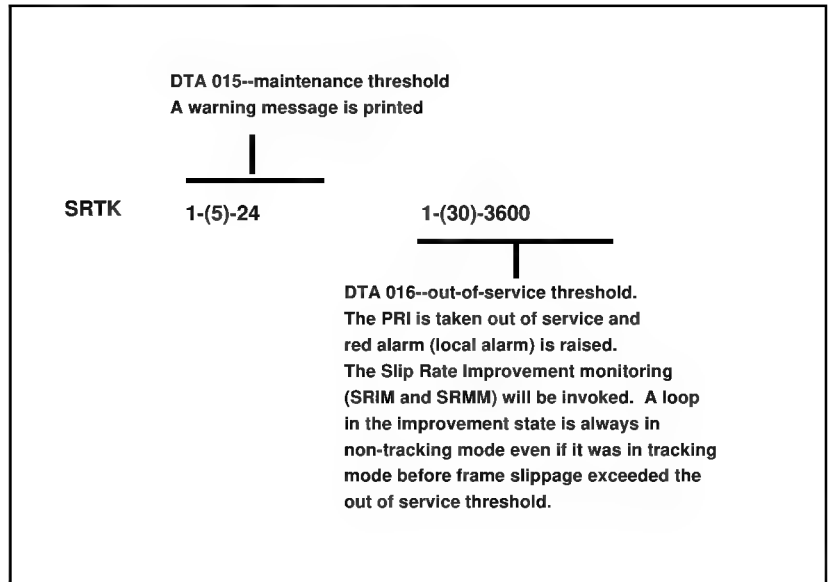
DTI/PRI hardware detects frame slips in tracking and free run modes. For tracking mode, running the midnight routines prints the number of overflows and clears the counter. For free run mode, running the midnight routines prints the number of frame deletions and repetitions and clears the counters.

Tracking mode

There are two thresholds set in LD 73 as described in the table below (see also Figure 69):

Prompt	Value	Meaning
SRTK	1-(5)-24 1-(30)-3600	Slip rate maintenance (in hours) and out-of-service threshold (per hour). These are the frame slip rate thresholds for the tracking mode. The first value is the maintenance threshold; the elapsed time (in hours) in which 2 frame slips occur (default is 2 slips in 5 hours). The second value is the out-of-service threshold; or the number of slips allowed in one hour (default is 30 slips in 1 hour). When a threshold is reached, a DTA messages is output as follows: DTA015:Frame slip --- tracking --- maintenance limit. DTA016:Frame slip --- tracking --- out of service limit.

Figure 69
Frame slip tracking thresholds

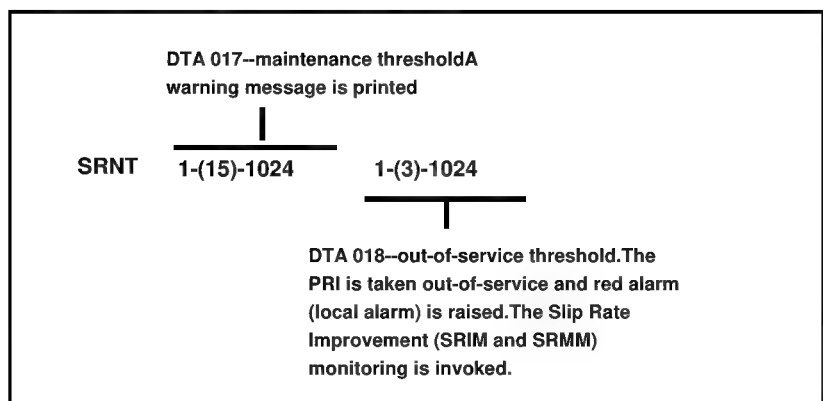


Free run (non-tracking) mode

A maintenance threshold and an out of service threshold are set in LD73 as described below (see Figure 70):

Prompt	Value	Meaning
SRNT	1-(15)-1024 1-(3)-1024	Non-tracking slip rate maintenance and out-of-service thresholds. These are frame slip rate thresholds for the non-tracking mode. The first value is the maintenance threshold in seconds, the amount of time in which 10 slips occur (default is 10 slips in 15 seconds). The second value is the out-of-service threshold in seconds, the amount of time in which 10 slips occur (default is 10 slips in 3 seconds). When these thresholds are reached, DTA messages are output.. Related DTA messages are described below. See Figure 70. DTA017:Frame slip --- free run (non-tracking) --- maintenance limit. DTA018:Frame slip --- free run (non-tracking) --- out of service limit.

Figure 70
Frame slip non-tracking thresholds



Frame slippage improvement timers

Once the frame slip out-of-service threshold has been reached, the DTI/PRI software will invoke a Slip Rate Improvement mechanism to monitor the slippage and return the DTI/PRI card to service if some criteria has been met. The criteria used to determine that the slip rate has improved enough to return a DTI/PRI card to service is that the maintenance threshold is exceeded less than M (SRMM — default 2) times in N (SRIM — default 1) minutes.

It is important to realize that this monitoring applies to both tracking and non-tracking modes. Note that a DTI/PRI card in the Slip Rate Improvement state is always in non-tracking mode, even if it was in tracking mode before frame slippage exceeded the out-of-service threshold.

There are two thresholds set in LD 73 as described in Figure 71:

Prompt	Value	Meaning
SRIM	(1)-127	Slip Rate Improvement time in minutes. After the tracking or non-tracking mode frame slippage out-of-service threshold is exceeded, the slip rate is monitored for improvement. If the non-tracking maintenance threshold exceeds SRMM or fewer times in the duration of this timer, then the trunks are returned to service. Otherwise, this timer is reset and monitoring continues.
SRMM	1-(2)-127	Slip Rate exceeded maintenance limit. Number of times the Slip Rate exceeds the maintenance limit while waiting for Slip Rate Improvement during the time window specified at the SRIM prompt. While waiting for Slip Rate Improvement one of three DTA messages is output as shown in Figure 71.

Figure 71
Frame slip improvement timers

SRIM	(1)-127
	DTA 026--frame slip out-of-service limit has been reached while monitoring frame slip improvement. Trunks remain out-of-service, and improvement timer is restarted. DTA 028--frame slip maintenance limit has been reached while monitoring frame slip improvement. Trunks remain out-of-service, and improvement timer is restarted. DTA 029-- frame slip improvement timer has expired, Slip Rate Improvement Criteria has been met. Trunks are being returned to service.
SRMM	1-(2)-127

Frame alignment

Loss of frame alignment occurs when the DTI/PRI card stops receiving the framing pattern on the DS-1 byte stream for a pre-defined period of time (3 seconds). See Figures 72 and 73. This condition can occur as a result of the far end of the T1 span going completely out-of service or any other reason resulting in losing the incoming DS-1 pulse stream.

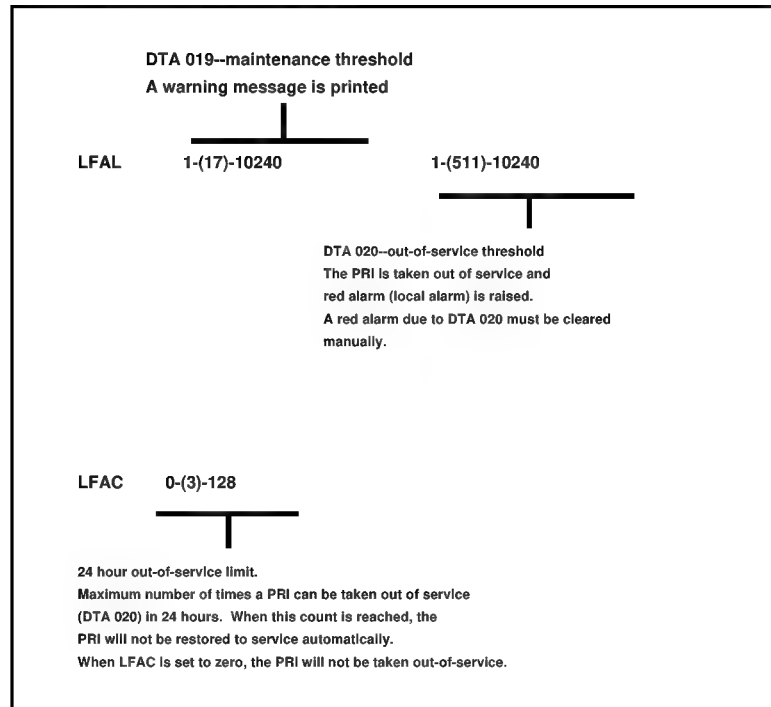
Loss of frame alignment thresholds

DTI/PRI hardware detects out of frame conditions. Running the midnight routines prints the number of occurrences when frame alignment was lost and clears the counters.

There are three frame alignment thresholds set in LD 73. When a maintenance or out of service threshold is reached, a DTA message is output as shown below.

DTA019	frame alignment maintenance limit
DTA020	frame alignment out of service limit

Figure 72
Frame alignment thresholds

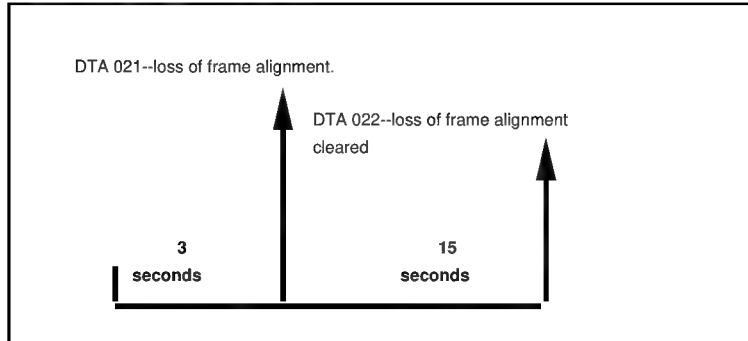


If a loss of frame alignment condition persists for 3 seconds, the affected DTI/PRI card is taken out of service and a red alarm (local alarm) is raised. See Figure 73.

If the loss of frame alignment condition clears at least 15 seconds, the DTI/PRI is automatically restored to service. The following DTA message is generated:

DTA021	loss of frame alignment has persisted for 3 seconds.
--------	--

Figure 73
Loss of frame alignment



Clock operation

The Option 11 system supports a single clock controller that can operate in one of two modes: tracking or non-tracking (also known as free-run).

Tracking mode

In tracking mode, one or possibly two DTI/PRI cards supply a clock reference to a clock controller daughterboard. When operating in tracking mode, one DTI/PRI is defined as the primary reference source for clock synchronization, while the other is defined as the secondary reference source (PREF and SREF in LD 73).

There are two stages to clock controller tracking:

- tracking a reference, and
- locked onto a reference.

When tracking a reference, the clock controller uses an algorithm to match its frequency to the frequency of the incoming clock. When the frequencies are very near to being matched, the clock controller is locked onto the reference. The clock controller will make small adjustments to its own frequency until both the incoming and system frequencies correspond.

If the incoming clock reference is stable, the internal clock controller will track it, lock onto it, and match frequencies exactly. Occasionally, however, environmental circumstances will cause the external or internal clocks to drift. When this happens, the internal clock controller will briefly enter the tracking stage. The green LED will flash momentarily until the clock controller is locked onto the reference once again.

If the incoming reference is unstable, the internal clock controller will continuously be in the tracking stage, with the LED flashing green all the time. This condition does not present a problem, rather, it shows that the clock controller is continually attempting to lock onto the signal. If slips are occurring, however, it means that there is a problem with the clock controller or the incoming line.

Free-run (non-tracking)

In free-run mode, the clock controller does not synchronize on any source, it provides its own internal clock to the system. This mode can be used when the Meridian 1 is used as a master clock source for other systems in the network. Free-run mode is undesirable if the Meridian 1 is intended to be a slave. It can occur, however, when both the primary and secondary clock sources are lost due to hardware faults or when invoked by using software commands.

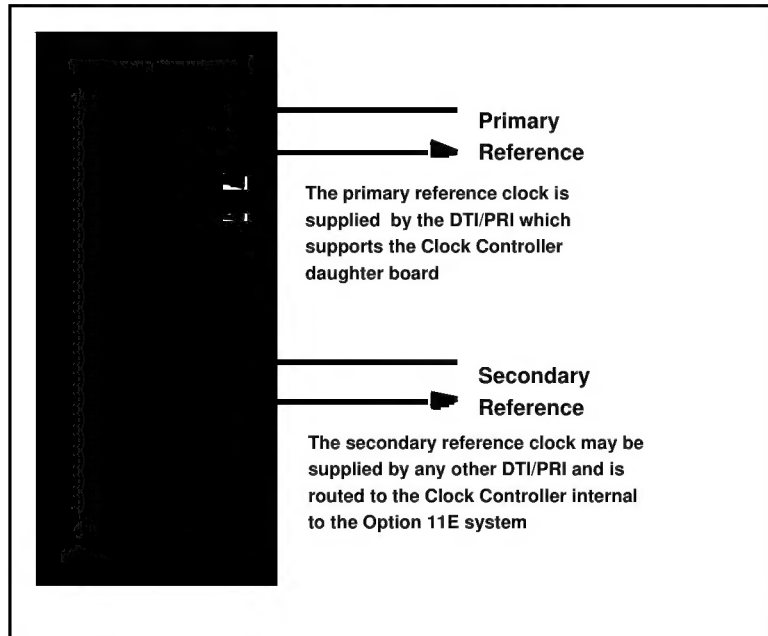
Reference clock errors

Meridian 1 software checks every 15 minutes to see if a clock controller or reference clock error has occurred.

In tracking mode, the clock controller is tracking on one reference clock. If a clock controller error is detected, or there is a problem with the reference clocks, the system will switch to free run mode.

A reference clock error occurs when there is a problem with clock driver or with the reference system clock at the far end. If the clock controller detects a reference clock error, with only one of the reference clocks, the reference clock is switched to the usable clock.

Figure 74
Clock controller primary and secondary tracking



Automatic clock recovery

Automatic switchover of the primary and secondary reference clocks is always *enabled* in the Option 11 system.

Note: EREF and MREF commands in LD 60, which control the enabling and disabling of automatic clock recovery, are not supported on the Option 11.

Replacing Equipment

Use the following procedures to replace the NTAK09, the NTAK20 and the NTAK93:

- 1 If the NTAK93 DCHI daughterboard is installed, first S/W disable the associated D-Channel (DCHI) using the following overlay and commands:

LD96 DIS DCH

Where X is the DCHI port number that was assigned in LD17).

- 2 If the NTAK20 Clock Controller daughterboard is installed, first S/W disable it using the following overlay and commands:

LD60 DIS CC 0

(Where CC is the card slot number of the NTAK09 that was supporting the NTAK20 Clock Controller).

- 3 S/W disable the DTI/PRI card as follows:

LD60 DISL X

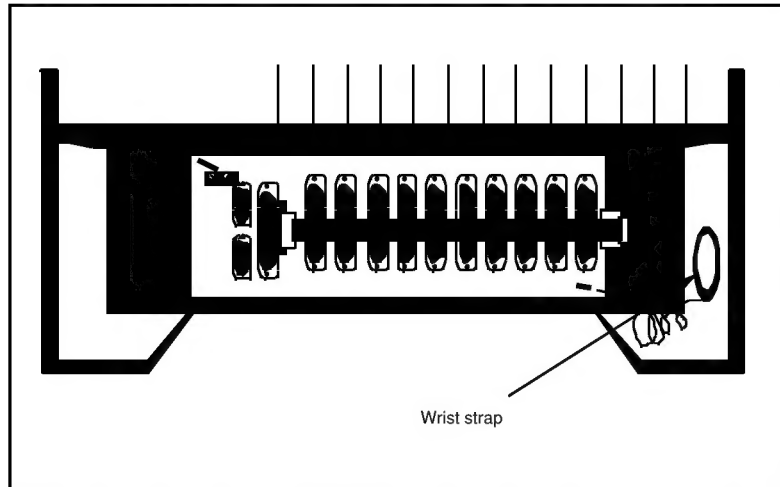
(Where X is the card slot number of the NTAK09 DTI/PRI).

- 4 Hold the NTAK09 by the lock latches, unlock the latches and slide the card out of the cabinet. Once out of the slot you may remove any of the daughterboards.

Note: To avoid damage to the circuit cards from electrostatic discharge, wear the wrist strap connected to the inside of your Option 11 cabinet whenever handling the circuit cards. Figure 75 shows the connection point for the wrist strap.

Note: Wrist strap connection to the Option 11 cabinet

Figure 75



- a** To remove the NTAK20 Clock Controller daughterboard, grasp the NTAK20 at opposite corners and gently “wiggle” it back and forth until all four corners are free. Be careful not to bend the connector pins.
 - b** To remove the NTAK93 Clock Controller daughterboard, grasp the NTAK93 at opposite corners and gently “wiggle” it back and forth until all four corners are free. Once the corners are free of the stand-offs, grasp the NTAK93 by its upper and lower right corners and slowly lift the right side of the NTAK93 up and away from the NTAK09 connectors, being careful not to bend any of the pins.
- 5** To replace the NTAK09 DTI/PRI card, NTAK20 Clock Controller or NTAK93 DCHI, refer to Chapter 4 PRI Implementation and Chapter 5 DTI Implementation as required. Be sure to set any switches and install any daughterboards as required.
- 6** Tag any defective or damaged equipment with a description of the problem and package it for return to a repair center.